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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
PATEL, ISHWARBHAI B				
ART UNIT		PAPER NUMBER		
2841				
NOTIFICATION DATE		DELIVERY MODE		
06/13/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/551,439

Applicant(s)

KATO, SHINOBU

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 April 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
4a) Of the above claim(s) 4, 6, 7, 10, 11 and 14-17 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 5, 8, 9, 12 and 13 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 29 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9/29/05, 6/21/07.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of specie I, claims 1-6 and 8-17 in the reply filed on April 28, 2008 is acknowledged. The traversal is on the ground(s) that the restriction lacks grounds upon which it can be evaluated whether the invention lack general inventive concept under PCT rule and further state that if the search and examination of all the claims in an application can be made without serious burden, the examiner must examine them on the merits, even though they include claims to independent or distinct invention. This is not found persuasive because as shown by various prior art cited in this rejection, multilayer printed wiring board with interlayer insulating layer and conductive layer on both or single side of a core substrate with power / ground via hole is old and known in the art. Further, full search of all the species with different structural arrangement is burdensome to the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on April 7, 2003. It is noted, however, that applicant has not filed a certified copy of the Japanese application as required by 35 U.S.C. 119(b).

Claim Objections

3. Claims 4, 6, 10, 11, 14, 15, 16 and 17 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims 4, 6, 10, 11, 14, 15, 16 and 17 are not been further treated on the merits.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-3, 5, 8, 9, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding claims 1 and 2, the recitation "an interlayer insulating layer and a conductive layer are formed on both sides or a single side of a core substrate having a plurality of through holes and electric connection is carried out through via holes" in confusing. The structure of the through holes and the via holes is unclear. As only one conductive layer is recited, it is further unclear the structure recited by "electric connection is carried out through via holes."

Claims 2-3, 5, 8, 9, 12 and 13 depend upon claim 1 and inherit the same deficiency.

Further:

Regarding claim 5, the recitation " in at least one of the ground **through holes** and the power **through holes, one or two or more through holes** are in a stack structure through entire layers up to the outermost layer" is confusing. The structure of stack structure of through hole and through hole is unclear.

Regarding claims 8 and 9, the recitation assuming that the thickness of the conductive layer on the core substrate is $\alpha 1$ and the thickness of the conductive layer on the interlayer insulating layer is $\alpha 2$, $\alpha 2 < \alpha 1 \leq 40 \alpha 2$, is unclear, as there is no conductive layer recited on the core substrate.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 5, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kanbe (US Patent No. 6,333,857).

Regarding claim 1, Kanbe in figure 2 discloses a multi-layer printed wiring board in which an interlayer insulating layer (121, figure 8) and a conductive layer (101,106) are formed on both sides or a single side of a core substrate (110) having a plurality of through holes (107) and electric connection is carried out through via holes (via holes above the core substrate, see figure 8), the through holes in the core substrate being

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disposed so that a ground through hole and a power through hole adjoin each other (see figure 10).

Regarding claim 2, Kanbe in figure 2 discloses multi-layer printed wiring board in which an interlayer insulating layer (121, figure 8) and a conductive layer (101,106) are formed on both sides or a single side of a core substrate (110) having a plurality of through holes (107) and electric connection is carried out through via holes (via holes above the core substrate, see figure 8), the through holes in the core substrate including two or more ground through holes and two or more power through holes (see figure 2), such that the ground through hole and the power through hole are disposed in a grid formation or in a staggered formation at adjacent positions (see figure 10).

Regarding claim 5, Kanbe further discloses at least one of the ground through holes and the power through holes, one or two or more through holes are in a stack structure through entire layers up to the outermost layer (see figure 8).

Regarding claim 12, Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three or more layers and including a thick conductive layer as an inner layer, and the conductive layer of each inner layer of the core substrate and the conductive layer of each surface are conductive layer for power layer or conductive layer for grounding (see figure 1 and 2).

Regarding claim 13, Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three layers and including a thick conductive layer as an inner layer, and the conductive layer of each inner layer of the core substrate is conductive layer for power layer or conductive layer for grounding (see figure 1 and 2) and the conductive layer on the front surface side is composed of signal line (via 107 is connected to signal line, figure 1).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe as applied to claim 1 above.

Regarding claim 3, Kanbe discloses all the features of the claimed invention as applied to claim 1 above but does not disclose a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm . However, the distance will be decided based on the space available in the board to avoid shorting of the adjacent pad on via during operation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Kanbe with a distance between the ground through hole and the power through hole is in a range of 60 to 550

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µm in order to avoid short circuit of the adjacent pad on via during operation to accommodate the via holes in the available space in the board.

11. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe as applied to claim 1 above, and further in view of Strandberg (US Patent No. 6,323,435).

Regarding claim 8 and 9, Kanbe discloses all the features of the claimed invention as applied to claim 1 but does not disclose the relationship between the conductive layer on the core substrate and on the insulating layer as recited in claims 8 and 9.

However, as disclosed by Strandberg in figure 1, it is known in the art to have the conductive layer formed in the buildup portion thinner than that the layer formed in the core substrate to have high density interconnect.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the conductive layer formed on interlayer insulating resin thinner than that of the layer in the core substrate, meeting the relationship as recited in claim 8 and 9, as taught by Strandberg, in order to have high density interconnect.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

It in figure 2 discloses a structure with conductive layer in the core substrate thicker than that on the interlayer insulating layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.